MONOLITHIC INDIUM PHOSPHIDE-BASED HEMT MULTIOCTAVE DISTRIBUTED AMPLIFIER

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ABSTRACT

The superior performance qualities of indium phosphide based High Electron Mobility Transistor (HEMT) structures has been established with discrete devices. In this paper, we report the first monolithic IC's made with this material system. Results are presented on a monolithic distributed amplifier with greater than 10 db gain from 2 to 30 GHz. At 14 GHz, the noise figure was 5.2 dB with 14 dB of associated gain. These circuits have all the necessary components for a high performance amplifier, including quarter micron EBL (Electron Beam Lithography) defined gates, MIM (Metal Insulator Metal) capacitors, air-bridge metal crossovers and plated-thru-substrate vias to the ground plane.

INTRODUCTION

The low noise and high gain properties of HEMT's have established them as the device of choice for low noise high gain analog applications extending to the millimeter wave regime. More recently, discrete HEMTs fabricated on MBE structures grown on InP substrates (1,2) have shown improved performance levels over traditional HEMT's grown on GaAs substrates. A logical extension of these developments is the application of these new devices in monolithic circuits that make use of the InP HEMTs superior characteristics. The implementation of monolithic circuits requires the development of passive components with fabrication techniques compatible with the InP material system. In the work reported here, we have developed a complete set of components that allow for design of microwave and millimeter wave monolithic circuits using this material. We have designed and tested a wide frequency bandwidth distributed amplifier.

DEVICE FABRICATION

The material used was a MBE-grown HEMT layer on an InP substrate. Figure 1 shows the ($Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$) HEMT structure used. Growth was carried out under conditions in which AlInAs is latticed matched to InP. A nucleation layer of AlInAs was chosen to promote smooth growth surface with minimum etch pit formation. A thicker lattice-matched GaInAs channel layer thickness was chosen to minimize the gate to drain capacitance C_{gd} with a slight decrease in transconductance (450 mS/mm). An undoped AlInAs layer was used near the surface to minimize gate leakage.

LAYER SEQUENCE

LAYER	MATRIX	X	T(Å)	DOPANT (CM^{-3})
CAP	GAINAS	.53	300	SI 3 X 10^{18}
BARRIER	ALINAS	.52	300	
CHARGE	ALINAS	.52	200	SI 1 X 10^{18}
SPACER	ALINAS	.52	20	
CHANNEL	GAINAS	.53	800	
BUFFER	ALINAS	.52	2500	
SUPERLATTICE (10X)	ALINAS GAINAS	.52 .53	25 25	
SUBSTRATE	INP		23 MILS	FE 1 X 10^{17}

Fig. 1 Layer structure of MBE grown wafer used in the present work. The layers grown are lattice matched to the indium phosphide substrate.

Except for the gate and backside via, all the fabrication steps were defined with standard projection lithography. Isolation was established by wet etching device mesas. Quarter micron gates were defined with a Cambridge Model 6.4 EBL machine. HEMTs were fabricated using wet etching to recess and self-align the gate; gate metal was Ti/Pt/Au; gate length was 0.25 μm at the contact point. The gate has a "mushroom" or "tulip" cross section to minimize its series resistance. Capacitors were built with 2000Å silicon nitride dielectric between two metallization steps. Air bridges were used at all metal crossovers to minimize unwanted parasitic capacitances. After completing the front side processing, the wafer was lapped and polished to 75 μm. Via holes were defined with a contact mask and then wet etched after which the entire back surface was then Au electroplated to establish a ground plane and to contact the front side metal wherever required.

AMPLIFIER DESIGN

Distributed amplifiers are characterized for their wide bandwidth (3) and, with proper design, flat response. The distributed amplifier reported here uses the 5 cells each in a cascode (4) configuration, which was chosen for improved amplifier response and inter-cell isolation. Each cell has two 150 μm transistors, one device in a common source gain block feeding a second one in a common gate configuration as an impedance transformer and isolator. The added complexity of the amplifier is compensated by the increased bandwidth and gain of the amplifier. Both the input and output transmission lines are terminated on chip. The amplifier in its present configuration is direct coupled, i.e., the input line is connected to all the gates of the gain transistor while the drain of the output transistor is connected to the

output transmission line. Bias circuits are included in the circuit with proper bypass characteristics. The amplifier was designed using microstrip transmission lines as signal paths to be directly matched to a 50 Ω system.

EXPERIMENTAL RESULTS

S-parameters of discrete transistors (on the same wafer and proximate to the amplifier) were measured with CASCADE™ probes. We have found excellent correlation of discrete device and amplifier performance, as predicted by standard nodal analysis. These on-wafer devices also serve as process monitors providing information on the effect of processing steps on the device performance. Representative performance of discrete HEMTs from the same wafer is shown in Fig. 2. U, MSG and H_{21}, calculated from the S-parameters, are plotted as function of frequency. By extrapolating the resulting curves for U and H_{21} with a 6 db/octave rolloff from the graph, F_{max} and f_t are found to be 200 GHz and 70 GHz, respectively. The transistor was 150 µm wide and it was biased at 2.25 V_{ds} and 26 ma I_{ds}. The extrinsic transconductance was 450 mS/mm. This is the same type of transistor that was used in the distributed amplifier.

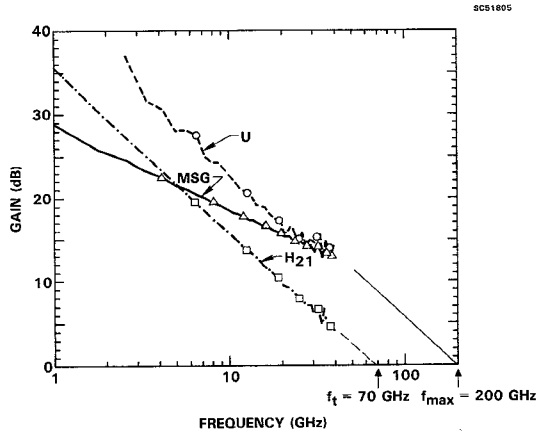

Fig. 2 Plot of U, H_{21} and MSG of a discrete device from the same wafer. The S-parameters were measured with a CASCADE™ RF probe to 40 GHz. By extrapolating U and H_{21} with a 6 db per octave rolloff, f_{max} and f_t can be calculated to be 200 GHz and 70 GHz, respectively.

Figure 3 shows a photograph of a fabricated five section distributed amplifier. The chip dimensions are 3 mm by 1.5 mm. Each section is made up of two 150 µm wide transistors in cascode configuration with the gate of the load transistor effectively AC bypassed by MIM capacitors to ground. The two transistors are connected in series (drain-1 to source-2), with input and output lines terminated to improve the input and output impedance. The amplifier was tested with a HP8510 network analyser in a 50 Ω system. Figure 4 shows the measured gain vs frequency for the amplifier, which operated at 3.9 V and 148 ma of total supply current. The amplifier operated over up to 8 V with less than a db decrease in the small signal gain. The gain was better than 10 db over the entire range to 30 GHz. Also shown in the same figure are the amplifier calculated theoretical response as

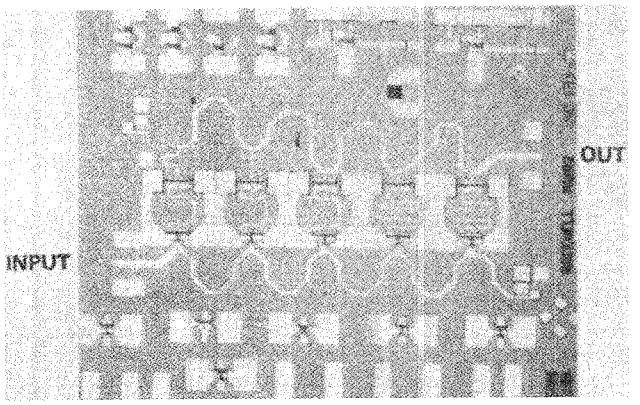

Fig. 3 Monolithic indium phosphide five section distributed amplifier. Each section consists of two transistors in Cascode configuration. The bias supplies are decoupled and the input (bottom) and output (top) lines are terminated.

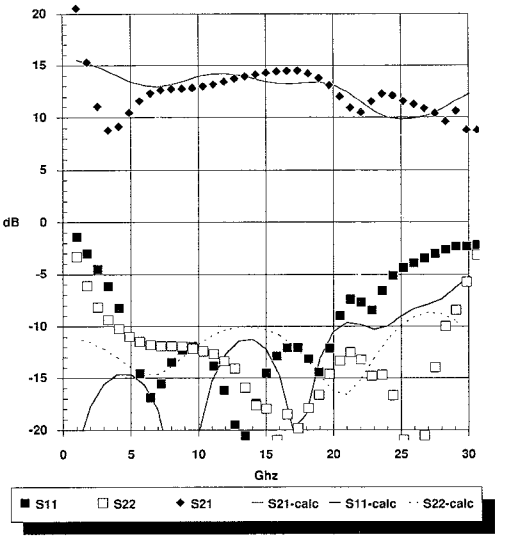

Fig. 4 Theoretical and measured S-parameters of the Distributed amplifier from 1 to 30 GHz. S_{12} was less than -30 db over the entire range and therefore out of scale in this plot. The voltage to the amplifier was 4.5 V and the total current 124 ma.

calculated by the Touchstone ("EEsof") program. The theoretical and experimental data agree very well in the region of interest. The noise figure of the amplifier from 12 to 18 GHz was measured with a HP8970B noise figure meter. Figure 5 shows the noise figure and associated gain of the amplifier from 12 to 18 GHz. As can be observed in the figure the amplifier was insensitive to a supply current increase of 20%. Discrete devices from the same wafer show excellent tuned single frequency noise figure typically 1.3 db with 8 db of associated gain at 35 GHz.

SUMMARY

The results of this paper demonstrate the compatibility of InP-based HEMTs with a MMIC implementation, with good yields and outstanding gain.

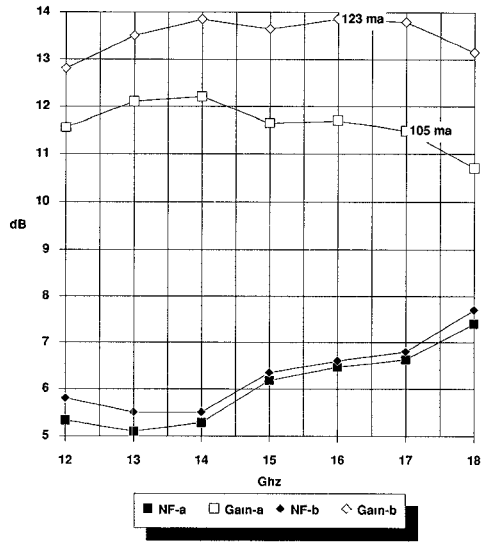

Fig. 5 Distributed amplifier noise figure for two different bias conditions.

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